FAIRCHILD SEMICONDUCTOR TM

June 1999

FDS6982

Dual N-Channel, Notebook Power Supply MOSFET

General Description

This part is designed to replace two single SO-8 MOSFETs in synchronous DC:DC power supplies that provide the various peripheral voltage rails required in notebook computers and other battery powered electronic devices. FDS6982 contains two unique 30V, N-channel, logic level, PowerTrench® MOSFETs designed to maximize power conversion efficiency.

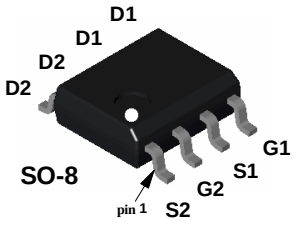
The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized for low conduction losses (less than 20mΩ at V_{GS} = 4.5V).

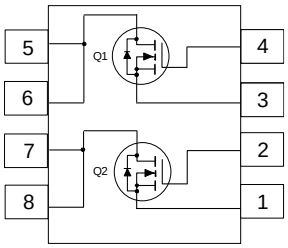
Applications

- Battery powered synchronous DC:DC converters.
- Embedded DC:DC conversion.

Features

- Q2: 8.6A, 30V. $R_{DS(on)}$ = 0.015 Ω @ V_{GS} = 10V
  $R_{DS(on)}$ = 0.020 Ω @ V_{GS} = 4.5V
- Q1: 6.3A, 30V. $R_{DS(on)}$ = 0.028 Ω @ V_{GS} = 10V
  $R_{DS(on)}$ = 0.035 Ω @ V_{GS} = 4.5V
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q2	Q1	Units
V_{DSS}	Drain-Source Voltage		30	30	V
V_{GSS}	Gate-Source Voltage		±20	±20	V
I_D	Drain Current - Continuous	(Note 1a)	8.6	6.3	A
	- Pulsed		30	20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS6982	FDS6982	13”	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

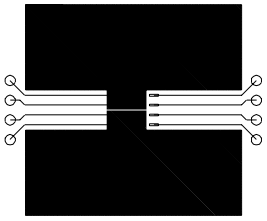
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	Q2 Q1	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	Q2 Q1		27 26		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	All			1	µA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	Q2 Q1	1 1	2.2 1.6	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	Q2 Q1		-5 -4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 8.6 A V_{GS} = 10 V, I_D = 8.6 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 7.5 A	Q2		0.012 0.018 0.016	0.015 0.024 0.020	Ω
		V_{GS} = 10 V, I_D = 6.3 A V_{GS} = 10 V, I_D = 6.3 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 5.6 A	Q1		0.021 0.038 0.028	0.028 0.047 0.035	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 8.6 A V_{DS} = 5 V, I_D = 6.3 A	Q2 Q1		50 40		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	Q2 Q1		2085 760		pF
C_{oss}	Output Capacitance		Q2 Q1		420 160		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		160 70		pF

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

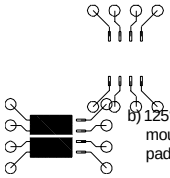
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω	Q2 Q1		15 10	27 18	ns
t_r	Turn-On Rise Time		Q2 Q1		11 14	20 25	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		36 21	58 34	ns
t_f	Turn-Off Fall Time		Q2 Q1		18 7	29 14	ns
Q_g	Total Gate Charge	Q2 V_{DS} = 15 V, I_D = 8.6 A, V_{GS} = 5 V	Q2 Q1		18.5 8.5	26 12	nC
Q_{gs}	Gate-Source Charge	Q1	Q2 Q1		7.3 2.4		nC
Q_{gd}	Gate-Drain Charge	V_{DS} = 15 V, I_D = 6.3 A,V_{GS} = 5 V	Q2 Q1		6.2 3.1		nC
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2 Q1			1.3 1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2) V_{GS} = 0 V, I_S = 1.3 A (Note 2)	Q2 Q1		0.72 0.74	1.2 1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.Thermal rating based on independant single device opperation.



a) 78° C/W when mounted on a 0.5 in^2 pad of 2 oz. copper.



b) 125° C/W when mounted on a 0.02 in^2 pad of 2 oz. copper.

c) 135° C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics: Q2

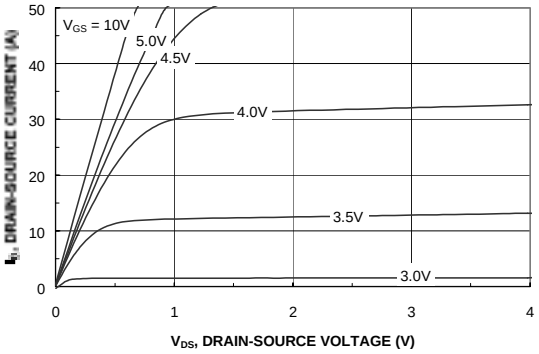


Figure 1. On-Region Characteristics.

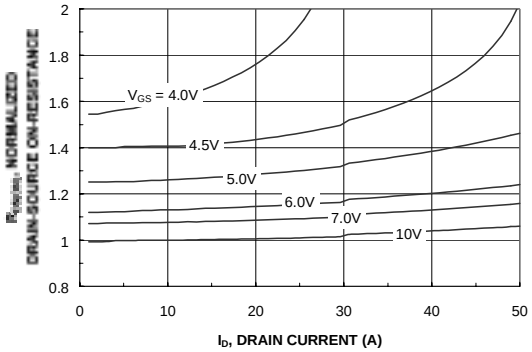


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

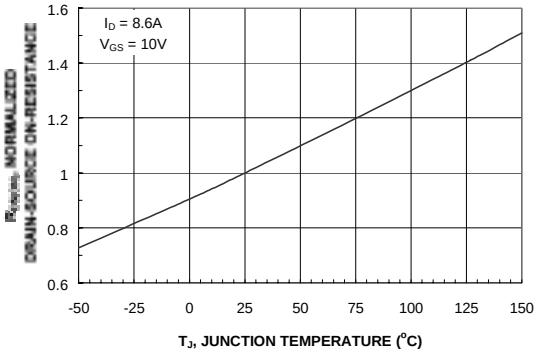


Figure 3. On-Resistance Variation with Temperature.

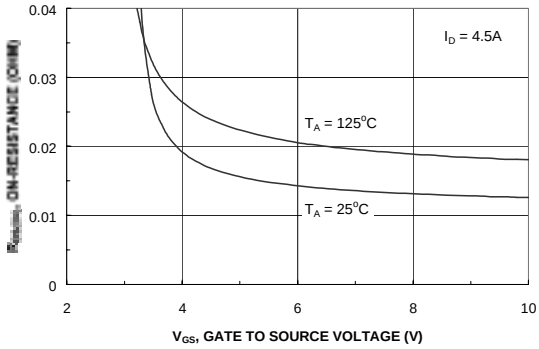


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

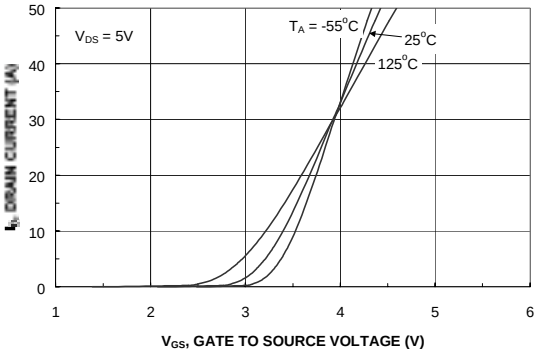


Figure 5. Transfer Characteristics.

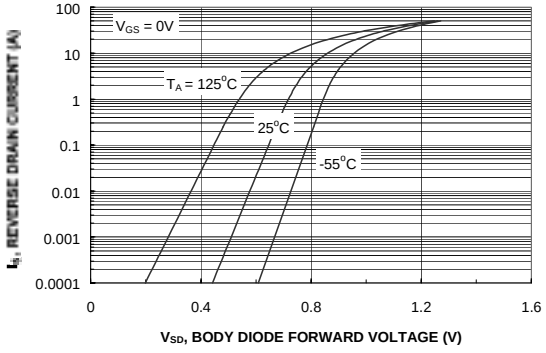


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2 (continued)

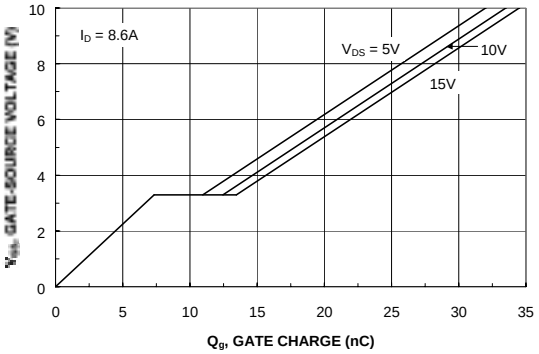


Figure 7. Gate-Charge Characteristics.

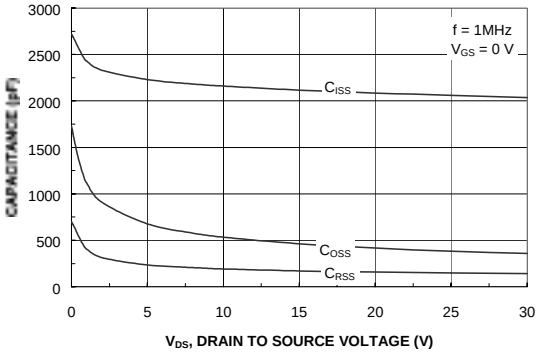


Figure 8. Capacitance Characteristics.

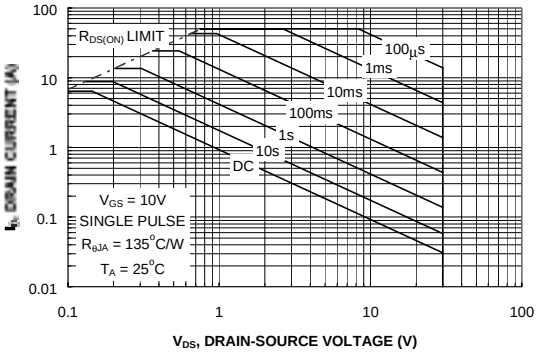


Figure 9. Maximum Safe Operating Area.

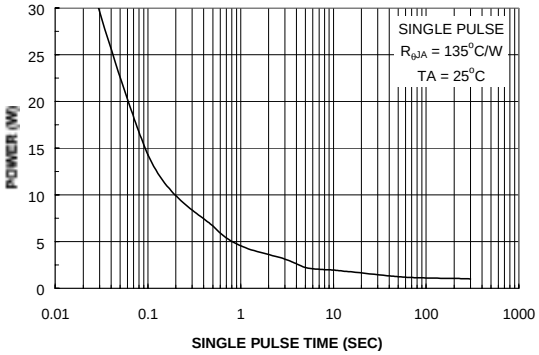


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1

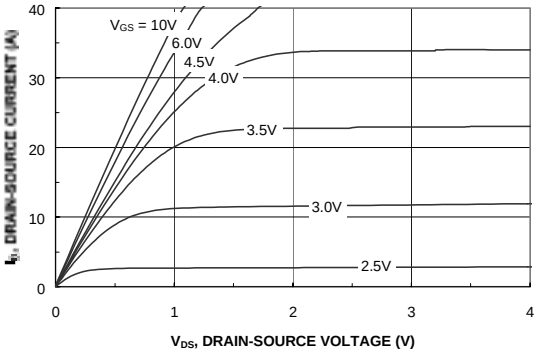


Figure 11. On-Region Characteristics.

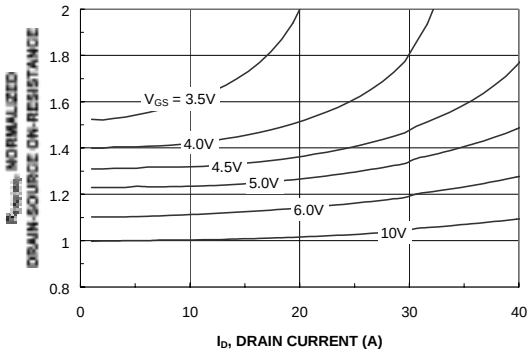


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

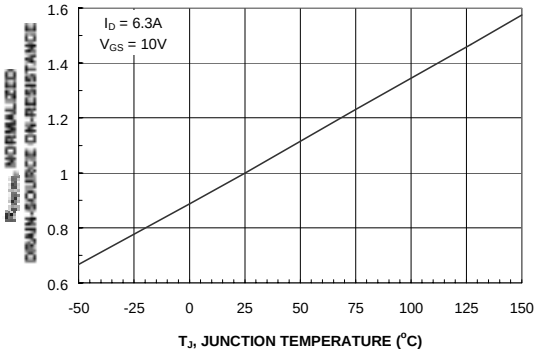


Figure 13. On-Resistance Variation with Temperature.

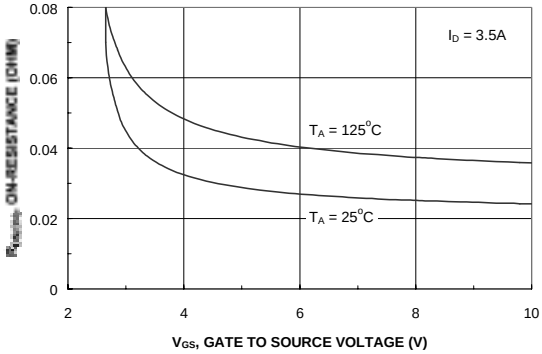


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

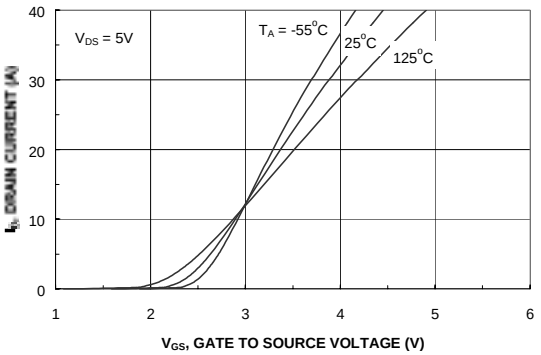


Figure 15. Transfer Characteristics.

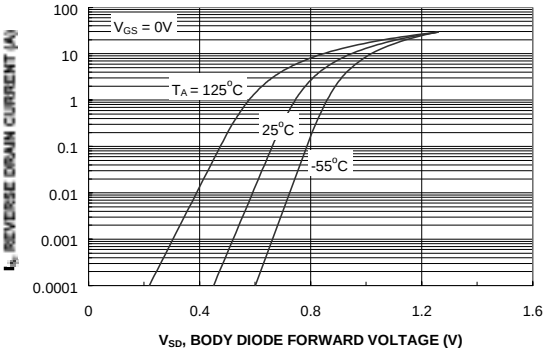


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1 (continued)

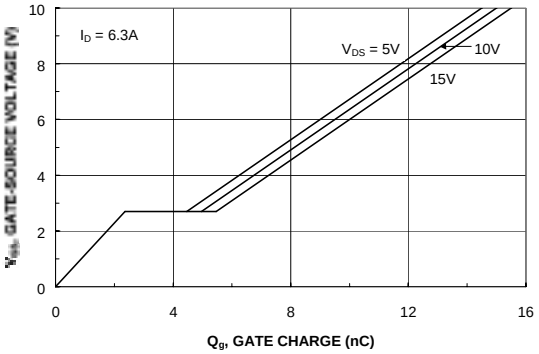


Figure 17. Gate-Charge Characteristics.

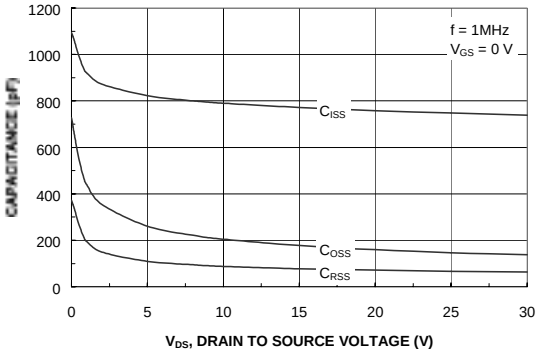


Figure 18. Capacitance Characteristics.

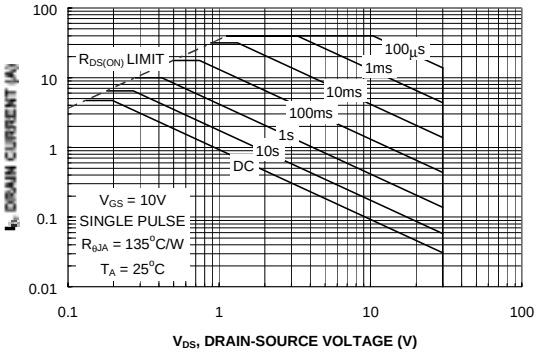


Figure 19. Maximum Safe Operating Area.

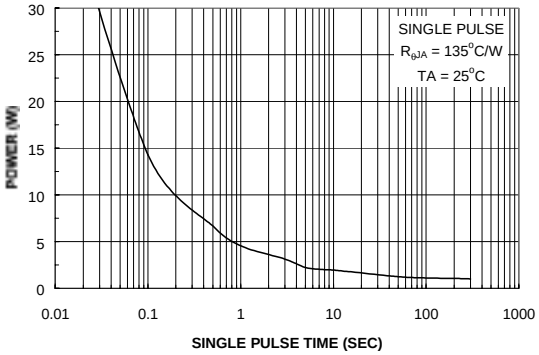


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1 & Q2 (continued)

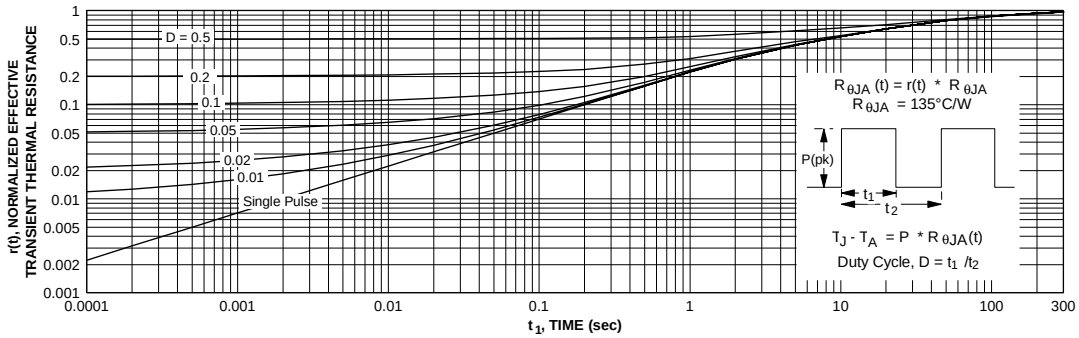


Figure 21. Transient Thermal Response Curve.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST ®	OPTOLOGIC™	SMART START™	VCX™
Bottomless™	FASTr™	OPTOPLANAR™	STAR*POWER™	
CoolFET™	FRFET™	PACMAN™	Stealth™	
CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E^2CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.